Serial No.: 10/619,989

REMARKS

These remarks follow the order of the paragraphs of the office action. Relevant portions of the office action are shown indented and italicized.

Claims 1-20 remain in the application. Claims 21 and 22 are added to protect a detailed embodiment of the invention.

DETAILED ACTION

Priority

1. Since the petition to have reference accepted under 37 CFR 1.78(a)(3) is granted, the amendment to the specification filed December 27, 2005 in accordance with 37 CFR 1.78(a)(3) is entered.

In response, applicants respectfully state their appreciation for the entering of the amendment.

Claim Objections

2. Claim 1-10, 17, 18 are objected to because of the following informalities: "moving the contents of the buffer to the payload portion of the control data block" on line 10 of claim 1 is not underlined, and therefore is not considered proper as added matter. Furthermore, line 8 of claim 1 already recites moving the contents of the buffer to the payload portion" and claim 1 appears to end at line 9 by the presence of a period.

In response, applicants respectfully state that claim 1 is amended to overcome the claim objection. Line 10, the non-underlined text after the period of line 9, is a typographic error and is deleted in that it is indeed not properly added matter. Claim 1 is allowable as amended and the objection to Claims 1-10, 17, 18 is overcome.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:
The specification shall contain a written description of the invention, and or the manner and process of making and using it, in such full, dear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.
The following is a quotation of the second paragraph of 35 U.S.C. 112:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Serial No.: 10/619,989

4. Claims 11-16. 19-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject mailer, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Page 40. lines 3-5 discloses "The payload portion comprises a plurality of fields each containing the identity of the LCP channel that indicated the completion event", It appears that the cited portion only supports a payload portion having a plurality of fields, each corresponding to one of the ports - rather than to a different one of the ports.

In the example of FIG. 18, there are 26 fields in the payload portion. Each field of payload portion contains the identity of the LCP channel (ports) that indicated the completion event (the interrupt) - hence a payload portion having a plurality of fields, each corresponding to one of the ports. The limitation "a plurality of fields each corresponding to a different one of the port" would require 28 different ports, and such limitation appears not to be supported by the specification.

Furthermore, it appears that there is no support for moving the contents of the buffer to the corresponding fields of the payload portion" - as page 38, lines 25-26 merely discloses "when preset conditions are met, an Interrupt Control Block (ICS) 1680 is generated by the ISOC 120 from the information stored in the interrupt FIFO 1660".

In response, applicants respectfully state that the specification is amended to include the matter in Claims 11-16. 19-20. This is done to meet the enablement requirement of 35 U.S.C. 112, since, any matter in the claims as originally filed is deemed to be old and proper matter. The amended portion of the specification clearly enables and supports method with a payload portion having a plurality of fields, each corresponding to a different one of the ports. This embodiment need not meet the criteria of the example of FIG. 18.

Furthermore, the amended specification for this embodiment also clearly supports "moving the contents of the buffer to the corresponding fields of the payload portion." This overcomes the rejection of Claims 11-16. 19-20 under 35 U.S.C. 112, first paragraph, and claims 11-16. 19-20 are allowable.

5. Claims 8-10, 17-20 are rejected under 35 USC. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Serial No.: 10/619,989

Claim 8 recites "A peripheral device comprising apparatus claimed in claim 1" in line 1. Since claim 1 also recites "a peripheral device" in line 2, it is not clear whether the peripheral device of claim 8 is the same as the peripheral device of claim 1.

In response, applicants respectfully state that claim 8 is amended to overcome the rejection under 35 USC. 112, second paragraph. Thus claim 8 is allowable.

Claim 9 recites 'A data communication network interface comprising a peripheral device as claimed in claim 8" in lines 1-2. Since claim 9 depends on claim 8, which depends on claim 1, it is not clear whether the peripheral device recited in claim 9 refers to the peripheral device recited in line 2 of claim 1, or the peripheral device recited in line 1 of claim 8 - if they are not the same. Furthermore, "apparatus" in line 1 of claim 8 should be replaced with the apparatus, and a peripheral device" in line 1 of claim 9 should be replaced with "the peripheral device".

In response, applicants respectfully state that claim 9 is amended to overcome the rejection under 35 USC. 112, second paragraph. Thus claim 9 is allowable.

Claim 17 recites A computer program product comprising a computer usable medium having computer readable program code means embodied therein for causing transfer of interrupts, the computer readable program code means...comprising computer readable program code means for causing a computer to effect the functions and all the limitations of claim 1". Since claim 1 is directed to an apparatus, the limitations of claim 1 pertain to the all elements of the apparatus of claim 1 It is not clear how a computer readable program code means can cause a computer to effect all the elements of an apparatus, how a computer program code means can comprise all the elements of an apparatus, or how a computer program product can comprise all the elements of an apparatus.

In response, applicants respectfully state that the language of claim 17 as originally claimed, used Beauregard claim language that has been used for years in many issued patents. It was amended to meet what was considered the specific requirement of the previous office communication. The comments of the present office communication are correct. Claim 17 is amended herein to overcome the rejection under 35 USC. 112, second paragraph. Thus claim 17 is allowable.

Claim 18 recites "A computer program product comprising a computer usable medium having computer readable program code means embodied therein for causing data processing, the computer readable program code means.., comprising computer readable program code means for causing a computer to effect the functions and all the imitations of claim 10'. Since claim 10 is directed to an apparatus, the limitations of claim 10 pertain to the all elements of the apparatus of claim 10. It is not clear how a computer

Serial No.: 10/619,989

readable program code means can cause a computer to effect all the elements of an apparatus, how a computer program code means can comprise al. the elements of an apparatus or how a computer program product can comprise all the elements of an apparatus.

In response, applicants respectfully state that the language of claim 17 as originally claimed, used Beauregard claim language that has been used for years in many issued patents. It was amended to meet what was considered the specific requirement of the previous office communication. The comments of the present office communication are correct. Claim 18 is amended herein to overcome the rejection under 35 USC. 112, second paragraph. Thus claim 18 is allowable.

Claim 19 recites "An article of manufacture comprising a computer usable medium having computer readable program code means embodied therein for causing transfer of interrupts, the computer readable program code means...comprising computer readable program code means for causing a computer to effect the steps and all the limitations of claim 11". It is not clear whether the article of manufacture comprises all the limitations of claim 11 or the computer readable program code means comprises all the limitations of claim 11, or a computer readable program code means causes a computer to effect all the limitations of claim 11. Further, it is not clear whether there is any distinction between steps and limitations - in line 4.

In response, applicants respectfully state that the language of claim 19 as originally claimed, used Beauregard claim language that has been used for years in many issued patents. It was amended to meet what was considered the specific requirement of the previous office communication. The comments of the present office communication are correct. Claim 19 is amended herein to overcome the rejection under 35 USC. 112, second paragraph. Thus claim 19 is allowable.

Claim 20 recites "A program storage device readable by machine, tangibly embodying a program of instructions.. to perform method steps for transferring interrupts, said method steps comprising the steps and all the limitations of claim 11". It is not clear whether there is any distinction between steps and limitations - in line 3. "machine" in line 1 should also be replaced with "a machine".

In response, applicants respectfully state that the language of claim 20 as originally claimed, used Beauregard claim language that has been used for years in many issued patents. It was amended to meet what was considered the specific requirement of the previous office communication.

Serial No.: 10/619,989

The comments of the present office communication are correct. Claim 20 is amended herein to overcome the rejection under 35 USC. 112, second paragraph. Thus claim 20 is allowable.

The rejections that follow are based on the examiners best interpretation of the claims.

Claim Rejections -35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentabilty shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. in considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject mailer of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyake et at (US 5,349,564) in view of Andrews et al. (USP 5,968,158) and further in view of Satran et at (USP 6,430,183).

In response, the applicant respectfully states that Claims 1 - 20 are apparently not made obvious by the combination of Miyake, Andrews and Satran. Applicants respectfully state that exception is taken with the alleged equivalence of elements in Claims 1-20 and .Miyake, Andrews and Satran. The office communication is reading into the cited art elements of the present claims where these do not exist. There is apparently use of common words and phrases in Miyake, Andrews and Satran and Claims 1-20. However the words and phrases are used in different combinations and different context in each.

The present invention, claimed in Claims 1 - 20, provides:

Methods, systems and apparatus for transferring interrupts from a peripheral device to a host computer system is described. In an example embodiment, an apparatus comprises a buffer for storing indications of interrupts generated by the peripheral device. In response to a preset condition being met, a controller generates a control data block having a payload portion, moves the contents of the buffer to the payload portion of the control data block, and sends the control data block to the host computer system.

Thus, the present invention, as claimed in claims 1-20, provides methods, systems and apparatus for transferring interrupts from a peripheral device to a host computer system.

Whereas, the cited art to Miyake, US Patent 5,349,564, filed: July 17, 1991, is entitled: "Multi-port RAM having means for providing selectable interrupt signals". The Miyake abstract reads :

"A multi-port RAM has a decoding portion for decoding a plurality of specific addresses for generating interruptions and a selection circuit for selecting some addresses from among the plurality of specific addresses. Since the plurality of addresses are selected for generating interruptions in parallel or in the sequence of time for each generation of an interruption, the data processing capability at the time of generation of interruptions can be improved".

Thus Miyake is concerned with "providing selectable interrupt signals." Miyake is apparently not concerned with "transferring interrupts from a peripheral device to a host computer system," as are claims 1-22.

The cited art to Andrews, US Patent 5,968,158, filed: October 6, 1997, is entitled: "Apparatus including a host processor and communications adapters interconnected with a bus, with improved transfer of interrupts between the adapters and host processor". The Andrews abstract reads :

"A pair of communications adapters each include a number of digital signal processors and network interface circuits for the attachment of a multi-channel telephone line. A bus connecting the communications adapters can carry data between a network line attached to one of the adapters and the digital signal processors of the other adapter. The digital

signal processors on each card are connected to a host, or controller, processor. Each digital signal processor interrupts its host processor by transmitting an interrupt control block as data to a data memory of the host processor, and by subsequently sending an interrupt causing the host processor to examine the data memory. Preferably, the interrupt control block includes data representing a number of requested interrupts."

Andrews is concerned with improved transfer of interrupts between communications adapters interconnected with a bus and a host processor. Thus, besides the art of Miyake, also the art of Andrews is apparently not concerned with "transferring interrupts from a peripheral device to a host computer system," as are claims 1-22.

The other cited art to Satran, US Patent 6,430,183, filed: July 31, 1998, is entitled: "Data transmission system based upon orthogonal data stream mapping". The Satran abstract reads :

"A data transmission system, including a plurality of transmitters for transmitting a stream of multiplexed packets over a broadband channel, the packets being constructed from a stream of variable length data blocks, each of the blocks originating from different sources. The system also includes a plurality of receivers for receiving the stream of packets from the broadband channel and reconstructing the stream of variable length data blocks. The data blocks are distributed over one or more packets. The packets also include a packet header having a source identifier (SID) for identifying the source of the packet, and the first of the packets further including a block header having a block identifier (BID) for identifying the data block being transmitted".

Satran is concerned with "transmitting a stream of multiplexed packets over a broadband channel." Thus, besides the art of Miyake and Andrews, also the art of Satran is apparently not concerned with "transferring interrupts from a peripheral device to a host computer system," as are claims 1-22. Thus claims 1-22 are allowable over the cited art combination.

Besides there is apparently no reason to make the combination of Miyake concerned with "providing selectable interrupt signals," with Andrews concerned with improved transfer of interrupts between communications adapters interconnected with a bus and a host processor,

and/or with Satran concerned with "transmitting a stream of multiplexed packets over a broadband channel," except in an attempt to allegedly find the elements in the present claims.

The office communication paragraph 8 above in the present application is relying on the cited art to make the present claims obvious. It is known and established patent practice that an office communication may not cite a combination in order to make rejection of a claim for obviousness if the making of the combination is not alluded to in at least one of the references. Otherwise a claim can be deemed obvious when it is really not obvious by finding multiple combinations to make all the elements of a claim. Support is required and herewith requested for any reason used for any obviousness rejection made by the office communication besides the cited art. The cited art individually or together do not perform the combination of steps and/or functions of claims 1-20.

In the absence of any indication in the cited art to make the combination, the office communication may not make the combination. The office communication is employing hindsight in an attempt to form the elements of claims 1-22. It is also apparent that even when the combination is made the invention in claims 1-22 is not made obvious. Thus claims 1-22 are allowable over the cited art combination.

9. As per claim 1, Miyake teaches an apparatus [interrupt circuit 4, FIG. 1] for interrupting a host computer system [CPU 2; FIG. 1] by indications of interrupts generated by ports of a peripheral device [RAM 3, FIG. 1; claims 1, 4]. the peripheral device having a plurality of ports [ports A, B, C - FIG. 1], the apparatus for transferring interrupts from the peripheral device to the host computer system cdl. 1, lines 13-15]. Miyake does not specifically teach a buffer for storing the indications of interrupts. Andrews teaches a buffer [a distributed buffer 68-0 to 68-7, FIG. 5] for storing indications of interrupts [INT BLOCK l- INT BLOCK N, FIG. 6; col. 10, lines 60-62] of a peripheral device [10, FIG. 1], and a controller 64-0, FIG. 5; DMA: col. 11, line 51] for, in response to a preset condition being met [col. 11, lines 8-4?]. generating a control data block [a DMA data block], and sending the contents of the buffer to the host computer system via one of the ports port connected to PCI BUS 48, FIG. 5] to reduce the overhead for processing the interrupts when compared to processing the interrupts individually [col. 1, tines 39-41] It would have been obvious to one of ordinary skill in the art at the time the invention was made to store the indications of interrupts in a buffer and to send the indications of interrupts to the host computer system when a preset

condition is met, as is taught by Andrews, in order to reduce the overhead for processing the indications of interrupts.

Miyake/Andrews essentially teaches transferring indications of interrupts from the buffer to the host computer system using DMA. instead of using a control data block comprising a payload portion having a plurality of fields each corresponding to one of the ports and a header portion having an identifier for identifying the control data block, moving the contents of the buffer to the fields of the payload portion, and sending the control data block to the host computer system via one of the ports.

Satran teaches a control data block (First Packet Type, FIG. 2] comprising a payload portion 220, 230, FIG. 2] having a plurality of fields [a plurality of block header [220, FIG, 2] and payload data [230, FIG. 2] sections: col. 5, lines 9-15] each corresponding to a data block lobe transmitted, and a header. portion (210, FIG, 2] having an identifier [211, FIG. 2] for identifying the control data block (col. 4, lines 17- 32], moving the contents of a buffer to the fields of the payload portion [data blocks to be transmitted originating from a single source: col. 4, lines 3-4], and sending the control data block to a receiver [140, FIG. 13 via a port of transmitter [110, FIG. l]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a control data block, as is taught by Satran, in order to transfer a plurality of indications of interrupts from the peripheral device to a host computer via the port connected to PCI BUS 48 - as an alternative to using DMA to transfer the plurality of indications of interrupts from the peripheral device to a host computer.

In response, the applicant respectfully states that exception is taken with the alleged equivalence of elements in Claim 1 and Miyake, Andrews, and the art of Satran . The office communication is reading into the cited art elements of the present claims where these do not exist. Claim 1 reads:

1. An apparatus comprising:

a buffer for storing indications of interrupts generated by ports of a peripheral device, the peripheral device having a plurality of ports, said apparatus for transferring interrupts from the peripheral device to a host computer system, and

a controller for, in response to a preset condition being met, generating a control data block comprising a payload portion having a plurality of fields each corresponding to a port and a header portion having an identifier for identifying the control data block, moving the contents of the buffer to the payload portion of the control data block, and sending the control data block to the host computer system via one of the ports.

A review of the cited portion of Miyake fails to show that Miyake refers to any of the elements of claim 1. Miyake does not allude to:

a peripheral device,

interrupts generated by ports of a peripheral device,

a buffer for storing indications of interrupts generated by ports of a peripheral device,

and certainly not to:

apparatus comprising a buffer for storing indications of interrupts generated by ports of a peripheral device

The office communication states:

> *Miyake teaches* an apparatus [interrupt circuit 4, FIG. 1] for interrupting a host computer system [CPU 2; FIG. 1] by indications of interrupts generated by ports of a peripheral device [RAM 3, FIG. 1; claims 1, 4]. the peripheral device having a plurality of ports [ports A, B, C - FIG. 1], the apparatus for transferring interrupts from the peripheral device to the host computer system cdl. 1, lines 13-15].

Even if Miyake would teach as alleged:

> an apparatus for interrupting a host computer system by indications of interrupts generated by ports of a peripheral device, the peripheral device having a plurality of ports, the apparatus for transferring interrupts from the peripheral device to the host computer system,

which indeed Miyake does not, this is not the function of the buffer or controller of claim 1. Miyake is not concerned with a peripheral device at all.

The office communication states:

> *Andrews teaches a buffer [a distributed buffer 68-0 to 68-7, FIG. 5] for storing indications of interrupts [INT BLOCK l- INT BLOCK N, FIG. 6; col. 10, lines 60-62] of a peripheral device [10, FIG. 1], and a controller 64-0, FIG. 5; DMA: col. 11, line 51] for, in response to a preset condition being met [col. 11, lines 8-47]. generating a control data block [a DMA data block], and sending the contents of the buffer to the host computer system via one of the ports port connected to PCI BUS 48, FIG. 5] to reduce the overhead for processing the interrupts when compared to processing the interrupts individually [col. 1, tines 39-41] It would have been obvious to one of ordinary skill in the art at the time the invention was made to store the indications of interrupts in a buffer and to send the indications of interrupts to the host computer system when a preset condition is met, as is taught by Andrews, in order to reduce the overhead for processing the indications of interrupts.*

Applicants respectfully state that neither Miyake or Andrews are concerned with a peripheral device. A dictionary search on August 1, 06, at URL http://www.webopedia.com/TERM/p/peripheral_device.html, defines peripheral device:

> A computer device, such as a CD-ROM drive or printer, that is not part of the essential computer, i.e., the memory and microprocessor. Peripheral devices can be external -- such as a mouse, keyboard, printer, monitor, external Zip drive or scanner -- or internal, such as a CD-ROM drive, CD-R drive or internal modem. Internal peripheral devices are often referred to as *integrated peripherals*. Also see I/O.

Whereas, Andrews is concerned with an adapter. URL http://www.webopedia.com/TERM/a/adapter.html, defines adapter:

> (1) Short for expansion board.
>
> (2) The circuitry required to support a particular device. For example, video adapters enable the computer to support graphics monitors, and network *adapters* enable a computer to attach to a network. Adapters can be built into the main circuitry of a computer or they can be separate add-ons that come in the form of expansion boards

Thus exception is taken with the alleged equivalency and or obviousness of or from the cited art and claim 1.

Exception is also taken with the statement regarding Satran in the office communication, which states:

> *Satran teaches a control data block (First Packet Type, FIG. 2] comprising a payload portion 220, 230, FIG. 2] having a plurality of fields [a plurality of block header [220, FIG, 2] and payload data [230, FIG. 2] sections: col. 5, lines 9-15] each corresponding to a data block lobe transmitted, and a header. portion (210, FIG, 2] having an identifier [211, FIG. 2] for identifying the control data block (col. 4, lines 17- 32], moving the contents of a buffer to the fields of the payload portion [data blocks to be transmitted originating from a single source: col. 4, lines 3-4], and sending the control data block to a receiver [140, FIG. 13 via a port of transmitter [110, FIG. L].*

A review of the Satran (First Packet Type, FIG. 2] , 220, 230, FIG. 2], col. 5, lines 9-15], col. 4, lines 17- 32], col. 4, lines 3-4], and [140, FIG. 13 via a port of transmitter [110, FIG. L], or even the entire text of Satran fails to show that Satran is concerned with a control data block in any way. Satran is not concerned with any control of blocks, and certainly not with:

generating a control data block,

an identifier for identifying the control data block,

moving the contents of the buffer to the payload portion of the control data block, or

sending the control data block to the host computer system via one of the ports.

Satran with or without Andrews and Miyake do not allude to make obvious, or can be used to one skilled in the art to make obvious the function of the controller of claim 1, "a controller for, in response to a preset condition being met, generating a control data block comprising a payload portion having a plurality of fields each corresponding to a port and a header portion having an identifier for identifying the control data block, moving the contents of the buffer to the payload portion of the control data block, and sending the control data block to the host computer system via one of the ports." Even if some words or phrases are in common in the art and claim 1, the function is certainly not common.

Thus claim 1 and all claims that depend thereupon are allowable over the cited art.

10. As per claims 2-4, Andrews teaches the preset condition comprising a determination that the buffer is full [col. 11, lines 22-27: with the predetermined limit being set to the size of the buffer); the preset condition comprising a determination that at least a predetermined plurality of indications is stored in the buffer and that a predetermined period has elapsed [col. 11, lines 35-40); the preset condition comprising a determination that at least one indication is stored in the buffer and that a predetermined period has elapsed {col. 11, line 28-35] 11.

In response, the applicant respectfully states that exception is taken with the alleged equivalence of elements in Claims 2-4 and the cited portions [col. 11, lines 22-27], [col. 11, lines 35-40), {col. 11, line 28-35] of Andrews . The office communication is reading into the cited art elements of the present claims where these do not exist. Claims 2-4 read:

2. (original) An apparatus as claimed in claim 1, wherein the preset condition comprises a determination that the buffer is full.

3. (original) An apparatus as claimed in claim 1, wherein the preset condition comprises a determination that at least a predetermined plurality of indications is stored in the buffer and that a predetermined period has elapsed.

4. (original) An apparatus as claimed in claim 1, wherein the preset condition comprises a determination that at least one indication is stored in the buffer and that a predetermined period has elapsed.

A review of the cited portions of Andrews shows that Andrews is actually not concerned with the preset conditions of claims 2-4. Thus claims 2-4 are allowable over the cited art for themselves and because each depends on allowable claim 1.

As per claim 5, Satran does not specifically teach the header portion comprising a count indicative of the number of indications included in the payload portion. Since it was known in the art at the time the invention was made to use a count in a header of a packet to indicate the number data blocks contained in the packet - for packets with multiple data blocks, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a count in the header portion of the control data block in order to indicate of the number of indications of interrupts included in the payload portion of the control data block.

In response, the applicant respectfully states that exception is taken with the alleged equivalence of elements in Claim 5 and Satran . The office communication is reading into and using the cited art to make elements of the present claims where these do not exist. Claim 5 reads:

5. (Previously presented) An apparatus as claimed in claim 1, wherein the header portion comprises a count indicative of the number of indications included in the payload portion.

A review of Satran shows that Satran is actually not concerned with the count condition of claim 5. It only may become obvious to one that reads the claim with hindsight. Thus claim 5 is allowable over the cited art for itself and because it depends on allowable claim 1.

12. <u>As per claim 6</u>, Satran does not teach the header portion comprising a time of day stamp Since it was known in the art at the time the invention was made to include a time of day stamp to keep track of the packet processing order to maintain coherency, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a time of day stamp in the header portion of the control data block in order to keep track of the order for processing the control data block.

In response, the applicant respectfully states that exception is taken with the alleged equivalence of elements in Claim 6 and Satran . The office communication is reading into and using the cited art to make elements of the present claims where these do not exist. Claim 6 reads:

6. (original) An apparatus as claimed in claim 1, wherein the header portion comprises a time of day stamp.

A review of Satran shows that Satran is actually not concerned with the header portion comprises a time of day stamp of claim 6. It only may become obvious to one that reads the claim with hindsight. Thus claim 6 is allowable over the cited art for itself and because it depends on allowable claim 1.

13. As per claim 7, Andrews teaches the buffer comprising a FIFO memory buffer [col. 10, line 60 - col. 11, line 7].

In response, the applicant respectfully states that exception is taken with the alleged equivalence of elements in Claim 7 and Andrews. The office communication is reading into the cited art elements of the present claims where these do not exist. Claim 7 reads:

7. (original) An apparatus as claimed in claim 1, wherein the buffer comprises a first in - first out memory buffer.

Andrews may have a buffer but Andrews does not have the buffer of claim 7. It only may become obvious to one that reads the claim with hindsight. Thus claim 7 is allowable over the cited art for itself and because it depends on allowable claim 1.

14. As per claim 8, Miyake teaches a peripheral device [RAMS, FIG. 1] comprising the apparatus [interrupt circuit 4, FIG, 1).

In response, the applicant respectfully states that exception is taken with the alleged equivalence of elements in Claim 8 and Miyake. The office communication is reading into the cited art elements of the present claims where these do not exist. Claim 8 reads:

8. (currently amended) A peripheral device comprising the apparatus as claimed in claim 1.

A review of Miyake shows that Miyake is actually not concerned with a peripheral device of claim 8. It only may become obvious to one that reads the claim with hindsight. Thus claim 8 is allowable over the cited art for itself and because it depends on allowable claim 1.

Serial No.: 10/619,989

15. As per claim 9, Miyake teaches the peripheral device communicating with processors 8A and 8B. Since it was known in the art at the time the invention was made for processors to communicate with a peripheral device over a network, it would have been obvious to one of ordinary skill in the art at the time the invention was made for the peripheral device to be comprised in a data communication network interface - in order to communicate with the processors over a network. 16.

In response, the applicant respectfully states that exception is taken with the alleged equivalence of elements in Claim 9 and Miyake. The office communication is reading into the cited art elements of the present claims where these do not exist. Claim 9 reads:

9. (currently amended) A data communications network interface comprising ~~a~~ the peripheral device as claimed in claim 8.

A review of Miyake shows that Miyake is actually not concerned with the peripheral device or a data communications network interface of claim 9. It only may become obvious to one that reads the claim with hindsight. Thus claim 9 is allowable over the cited art for itself and because it depends on allowable claim 1.

As per claim 10, Miyake teaches an apparatus [1 FIG. 1] comprising a host processing system [2, FIG. 1] having a memory (3, FIG. 1], a data communications interface [ports A, B, C - FIG. 1) for communicating data between the host computer system through port A] and a data communications network [see rejection of claim 9 above] forming a data processing system FIG. 1] for controlling flow of interrupts from the data communication interface to the memory of the host computer system.

In response, the applicant respectfully states that exception is taken with the alleged equivalence of elements in Claim 10 and Miyake. The office communication is reading into the cited art elements of the present claims where these do not exist. Claim 10 reads:

10. (Previously presented) An apparatus as claimed in claim 1, further comprising:
a host processing system having a memory, a data communications interface for communicating data between the host computer system and a data communications network, forming a data processing system for controlling flow of interrupts from the data communication interface to the memory of the host computer system.

A review of Miyake shows that Miyake is actually not concerned with the data communications network interface of claim 10. The cited portion of Miyake [ports A, B, C - FIG. 1), do not make the data communications interface for communicating data between the host computer system and a data communications network, of claim 10. Miyake is certainly not concerned with and does not allude or make obvious to one skilled in the art, the element of "forming a data processing system for controlling flow of interrupts from the data communication interface to the memory of the host computer system, of claim 10." It only may become obvious to one that reads the claim with hindsight. Thus claim 10 is allowable over the cited art.

17. As per claim 11, claim 11 generally corresponds to claim 1, for a specific instance where the buffer contains only one indication of interrupt per port - for a plurality of pods, and the payload portion contains only a number of fields corresponding to the number of ports, each field of the payload portion would correspond to a different one of the ports, and the contents of the buffer are moved to the corresponding fields of the payload portion.

In response, the applicant respectfully states that exception is taken with the alleged equivalence of elements in Claims 1 and 11 with Miyake, Andrews, and the art of Satran . The office communication is reading into the cited art elements of the present claims where these do not exist. Claim 11 reads:

1. A 11. (original) A method comprising transferring interrupts from a peripheral device to a host computer system, the peripheral device having a plurality of ports, the step of transferring interrupts comprising:

storing interrupts generated by ports of the peripheral device in a buffer;

determining if a preset condition is met, and, in response to the preset condition being met;

generating a control data block comprising a payload portion having a plurality of fields each corresponding to a different one of the ports and a header portion having an identifier for identifying the control data block;

moving the contents of the buffer to the corresponding fields of the payload portion; and

sending the control data block to the host computer system via one of the ports.

As indicated for claim 1, claim 11 is similarly not made obvious by the cited art to one skilled in the art. A review of the cited portion of Miyake fails to show that Miyake refers to any of the elements of claim 11. Miyake does not allude to:

a peripheral device,
interrupts generated by ports of a peripheral device,
storing interrupts generated by ports of the peripheral device in a buffer;
determining if a preset condition is met,
generating a control data block
an identifier for identifying the control data block;
moving the contents of the buffer to the corresponding fields of the payload portion; or
sending the control data block to the host computer system via one of the ports.

These are all elements of claim 11. In particular, none of the cited art refers to a specific instance where the buffer contains only one indication of interrupt per port - for a plurality of pods, and the payload portion contains only a number of fields corresponding to the number of ports, each field of the payload portion would correspond to a different one of the ports, and the contents of the buffer are moved to the corresponding fields of the payload portion.

Applicants respectfully state that neither Miyake or Andrews are concerned with a peripheral device. Andrews is concerned with an adapter. Exception is also taken with the statement regarding Satran in the office communication. A review of the Satran (First Packet Type, FIG. 2] , 220, 230, FIG. 2], col. 5, lines 9-15], col. 4, lines 17- 32], col. 4, lines 3-4], and [140, FIG. 13 via a port of transmitter [110, FIG. L], or even the entire text of Satran fails to show that Satran is concerned with a control data block in any way. Satran is not concerned with any control of blocks, and certainly not with:

generating a control data block,

an identifier for identifying the control data block,

moving the contents of the buffer to the payload portion of the control data block, or

sending the control data block to the host computer system via one of the ports.

Satran with or without Andrews and Miyake do not allude to make obvious, or can be used to one skilled in the art to make obvious the function of the controller of claim 1, "a controller for, in response to a preset condition being met, generating a control data block comprising a payload portion having a plurality of fields each corresponding to a port and a header portion having an identifier for identifying the control data block, moving the contents of the buffer to the payload portion of the control data block, and sending the control data block to the host computer system via one of the ports." Even if some words or phrases are in common in the art and claim 1, the function is certainly not common.

Thus claim 11 and all claims that depend thereupon are allowable over the cited art.

18. As per claims 12-20, claims 12-16 generally correspond to claims 2-5,7 - and are rejected on the same basis as claims 2-5. 7; claim 17 generally corresponds to claim 1, and is rejected on the same basis as claim 1; claim 18 generally corresponds to claim 10. and is rejected on the same basis as claim 10; claims 19-20 generally correspond to claim 11, and are rejected on the same basis as claim 11.

In response, the applicant respectfully states that exception is taken with the alleged equivalence of elements in Claims 12-20 and Miyake, Andrews, and the art of Satran . The office communication is reading into the cited art elements of the present claims where these do not exist.

Since claims 12-16 are deemed by the office communication to generally correspond to claims 2-5, 7, the comments of the allow-ability of claims 2-5, 7, are applicable to claims 12-16.

Since claim 17 are deemed by the office communication to generally corresponds to claim 1, the comments of the allow-ability of claim 1 is applicable to claim 17.

Since claim 18 are deemed by the office communication to generally corresponds to claim 10. the comments of the allow-ability of claim 1 is applicable to claim 18.

Since claims 19-20 are deemed by the office communication to generally correspond to claim 11, the comments of the allow-ability of claim 11 are applicable to claims 19-20.

Response to Arguments

19. Applicant's arguments filed December 27, 2005 have been frilly considered but they are not persuasive or moot in view of the new grounds of rejections.

20. With respect to the claim rejections under 35 USC 112, applicant cited Various communication protocols can be supported simultaneously, with each protocol using a different LCP port', and argued that when there are many protocols, there are many different ports. 28 protocols would have 28 different ports.
The argument is not persuasive because page 40. lines 3-5 discloses "The payload portion comprises a plurality of fields each containing the identity of the LCP channel that indicated the completion event". Such disclosure does not require each of the plurality of fields to correspond to a different one of the ports. It merely requires each of the plurality of fields to correspond to a port. The 28 fields of FIG. 18 do not have to correspond to 28 different ports.
Furthermore, Various communication protocols can be supported simultaneously, with each protocol using a different LOP port" merely means that several ports can be used simultaneously. Such citation does not require the 28 fields to correspond to 28 different protocols.

In response, the applicant respectfully states that the specification is amended herewith to include text to show that the present invention includes a case "when there are many protocols, there are many different ports."

21. With respect to the 103 rejections and the teachings of Andrews, applicant's argument is somewhat confusing. It appears that applicant argued that Andrews does not teach a buffer for storing indications of interrupts generated by ports of a peripheral device. The arguments are moot in view of the new grounds of rejections.

In response, applicants respectfully state that Andrews is indeed not concerned with a peripheral device or ports of a peripheral device. Andrews is concerned with an adapter. Thus applicants

maintain that Andrews does not teach a buffer for storing indications of interrupts generated by ports of a peripheral device.

22. With respect to the 103 rejections and the teachings of Satran, applicant's argument is also confusing. It appears that applicant argued that the blocks of Satran are not "control data blocks" in claims 1-20, and that the control data block has "a payload portion".

As Satran teaches a control data block having a payload portion [FIG. 2] and applicant failed to show how the control data block in Satran is different from the control data block in applicant's invention, applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

It also appears that applicant also argued bodily incorporation of the references and/or argued against the references individually. The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the lest is what the combined teachings of the references would have suggested to those of ordinary skill in the art.

See In to Keller, 642 F.2d 413,208 USPQ 871 (CCPA 1981). Furthermore, one cannot show non obviousness by attacking references individually where the rejections are based on combinations of references. See In to Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); In to Merck & Co., 800 F.2d 1091,231 USPQ 375 (Fed. Cir. 1986).

In response, the applicant respectfully states that exception is taken with the alleged equivalence of elements in the Claims and Miyake, Andrews, and the art of Satran. The office communication is reading into the cited art elements of the present claims where these do not exist. The blocks of Satran are not the control data blocks of the claimed invention. Satran is apparently not concerned with control.

When a rejection is made for obviousness it must meet the criteria for obviousness. If it depends on cited art, the cited art must allude to the elements made obvious. If an obviousness rejection is made for other reasons, the office communication should support the other reasons. The use of cited art in a way not supportive of the alleged knowledge of those skilled needs the cited art to make the support. Otherwise hindsight is apparently used.

23. With respect to the 103 rejections and the motivation to combine, applicant argued there is no reason to combine Satran with Andrews, which are apparently unrelated art,

except for hindsight. It also appears that applicant argued that the suggestion to combine must be expressly suggested in any one or all of the references.

In response to applicants argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the revel of ordinary skill at the time the claimed invention was made, and does not include, knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See In re McLaughlin, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

In response to applicants argument that Andrews arid Satran are non-analogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See In to Oetiker, 977 F.2d 1443,24 USPQ2d 1443 (Fed. dr. 1992). In this case, both Andrews and Satran are concerned with how to send data from a source to a destination.

Applicant is also off the mark in arguing that the suggestion to combine must be expressly suggested in any one or all of the references. The measure is what the teachings of the references would suggest to one of ordinary skill in the art, not what the references specifically suggests. See In re Oetiker, 24 USPQ2d 1443 (Fed. dr. 1992).

In response, applicants respectfully state that a review of In re Oetiker, 24 USPQ2d 1443 (Fed. dr. 1992) apparently doesn't support the office communication statement above. In re Oetiker is apparently not concerned with what combination of art may be cited to invalidate a claim for obviousness. In re Oetiker concludes;

CONCLUSION

First, by concluding that the Wall declaration addressed an issue of law instead of an issue of fact, and second, by failing to articulate adequate reasons to rebut the Wall declaration, the examiner and Board failed to consider the totality of the record for the purpose of issuing a final rejection and thus erred as a matter of law. We are not in a position, however, to determine whether the specification contained an adequate written description of the claimed IFN-_ sequence. That determination requires, in the first instance, further proceedings in which the Wall declaration is addressed in a manner that is consistent with this opinion. The case is remanded to the Board for such further proceedings. See In re Beaver, 893 F.2d 329, 13 USPQ2d 1409 (Fed. Cir. 1989) (vacating Board's decision for failing to review all the appealed claims in accordance with the relevant regulations).

This is apparently not relevant to the present circumstance. The office communication in the present application is relying on the cited art to make the present claims obvious. Paragraph 8 of the office communication is reproduced below

8. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyake et at (US 5,349,564) in view of Andrews et al. (USP 5,968,158) and further in view of Satran et at (USP 6,430,183).

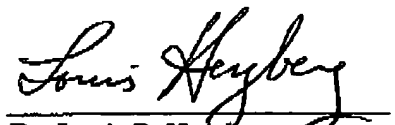
It is known and established patent practice that an office communication may not cite a combination in order to make rejection of a claim for obviousness if the making of the combination is not alluded to in at least one of the references. Otherwise a claim can be deemed obvious when it is really not obvious by finding multiple combinations to make elements of a claim. Support is required and herewith requested for any reason used for any obviousness rejection made by the office communication besides the cited art. The cited art individually or together do not perform, allude to or make obvious the combination of steps and/or functions of claims 1-20.

Thus claims 1-20 are allowable over the cited art. Claims 21 and 22 are detailed claims and are allowable even if each separate element is known, which they are not, since a new and novel combination of known elements are patentable.

It is anticipated that this amendment bring the application to allowance of all claims 1-20. In the event that any questions remain please contact the undersigned.

Please charge any fee necessary to enter this paper to deposit account 50-0510.

Respectfully submitted,

By: 

Dr. Louis P. Herzberg
Reg. No. 41,500
Voice Tel. (845) 352-3194
Fax. (845) 352-3194

3 Cloverdale Lane
Monsey, NY 10952

Customer Number: 54856